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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,432	12/28/2001	Alain Benayoun	FR920000066US1	1930

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EXAMINER	
LEVITAN, DMITRY	

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,432	BENAYOUN ET AL.	
	Examiner	Art Unit	
	Dmitry Levitan	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

1. The drawings are objected to because:

   a. Some functional blocks on Fig. 3-8 lack descriptive labels/names.

   b. Quality of the connections shown on Fig. 8 is not acceptable.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 1-15 are objected to because of the following informalities: claim 1 limitation "a memory block located at each of the cross points" is unclear, because memory location seems to

be irrelevant in the claim, contrary to the memory connection/association to the ports as claimed. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 limitation "a plurality of input ports and a plurality of output ports both being respectively connected to the plurality of LAN adaptors, each pair of input and output ports defining a cross point within the packet switch point" is unclear, because it is not understood what output and input ports are considered a pair and what is a cross point.

Claims 1 and 2 limitation "forwarding ... at each clock time" is unclear, because it is not understood when the forwarding should occur, as there are no time units are associated with "each clock time".

Claim 1 limitation "a data controller which forwards to the output port a data packet stored in a data memory unit of a memory block corresponding to the output port" is unclear, because it is not understood what is corresponding to the output port: a data packet or a memory block.

5. Claim 11 recites the limitation "the fourth memory controller" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4 and 11 are rejected (as best understood) under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (US 6,205,145).

7. Regarding claim 1, Yamazaki teaches a data transmission system having a plurality of networks interconnected by a hub (Switch fabric on Fig. 1 interconnected with variable length frame networks, shown on Fig. 1 and 1:13-40) including a plurality of adapters respectively connected to the plurality of networks (portions of termination nodes N1-N6 on Fig. 9 and 10 9:25-45), comprising:

A packet switch interconnecting the plurality of LAN adapters wherein a packet transmitted by any of the adapters to the packet switch (fabric F1 on Fig. 9 or a combination of fabrics on F1-F3 on Fig. 10) includes a header containing at least the address of the adapter to which the packet is forwarded (each of termination nodes N1 –N4, knows the nodes ID of the other termination nodes and transfers a frame with Destination Identifier field 610 on Fig. 11 as disclosed on 9:9:45-10:15), the packet switch includes a plurality of input ports and corresponding plurality of output ports both being respectively connected to the plurality of the adapters (packet switch on Fig. 5 having a plurality of input and output ports interfaces 10-13 connected to the plurality of

adapters 6:50-7:15), each pair of input port and output port defining a cross point (cross point is interpreted as combination of input and output data buffer means 20-23 and 30-33 on Fig. 5 for each existing connection between terminal nodes);

The packet switch comprises:

A memory block at each cross point for storing any data packet that is received from the input port corresponding to the cross point and which is to be forwarded to the output port corresponding to the cross point (input data buffer means 20-23 and cell producing means 40-43 on Fig. 5 to store input data 7:18-27), and

A memory block at each cross point includes a data memory unit for storing a data packet (storing the received packet in input buffer 120 on Fig. 8 and 8:33-60) and first memory controller which determines from the packet header whether the packet is to be forwarded to the output port associated with the cross point (control sections 144 and 143 and cell producing section with port ID register on Fig. 8 and 8:62-9:10) and storing the packet (in input buffer 120 on Fig. 8), a data controller which forwards to the output port a data packet stored in a data memory unit of a memory block corresponding to the output port at each clock time (portions of control section 143 and 170 on Fig. 8 and 10:26-36, forwarding stored data packets to the corresponding output port 10:14-26 under each clock/frame time indicated by a flag register on Fig. 20 and 21, 14:55-15:5, in the absence of congestion 8:27-32).

Yamazaki does not teach networks as LANs and locating memory blocks at each cross point.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add LANs and locating memory blocks at each cross point to the system of Yamazaki to incorporate well known and popular type of networks in the system, as many LANs

use Ethernet standard, which comprises variable length frames as utilized in the system and locate the memory blocks at the cross points to reduce the system delay by locating the memory blocks closer to the cross points.

8. Regarding claim 2, Yamazaki teaches the data controller includes a scheduler associated with each output port for selecting at each clock time a memory block among all memory blocks corresponding to the output port and causing the memory block to forward the data packet stored in the data memory unit to the output port when the predetermined criteria are met (congestion control means 70 on Fig. 5 managing frame construction means 50-53 and therefor output data buffer means/memory block 8:27-32, wherein a reconstructed frames are forwarded from the output data buffers 30-33 to the output ports 10-13 under each clock/frame time indicated by a flag register on Fig. 20 and 21, 14:55-15:5, in the absence of congestion 8:27-32).

9. Regarding claim 4, Yamazaki teaches an output data block connected to each output port for storing a data packet received from any memory block and transmitting the data packet to the output port under the control of the scheduler (output buffer 130 on Fig. 8 connected with output ports through interface control section 110 on Fig. 8 and transmitting the data packets under the control of the scheduler as shown in claim 2 rejection).

10. Regarding claim 11, Yamazaki teaches an overflow signal from the memory block to the scheduler when the memory block overflows (input buffers 40-43, shown on Fig. 5, requirement signal from buffer means 430 to the congestion control means 70 on Fig. 6 and 7:62-67).

11. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Takeuchi (US 5,233,603).

Yamazaki substantially teaches the limitations of the parent claims of claims 6 and 7.

Yamazaki does not teach an input control block, comprising an input memory unit, connected to each input port for buffering a data packet before transmitting the data packet over a distribution bus connected to all memory blocks corresponding to the input port and a third memory controller storing the packets into the input memory unit and reading them out over the bus.

Takeuchi teaches an input control block, comprising an input memory unit, connected to each input port for buffering a data packet before transmitting the data packet over a distribution bus connected to all memory blocks corresponding to the input port and a third memory controller storing the packets into the input memory unit and reading them out over the bus (multiplexer 202 on Fig. 3 comprising input buffers 1401-140N on Fig. 4 connected by a distribution bus 142 to buffer units 2501-250N 5:62-6:11, wherein data packets are stored at buffers 1401-140N and read out over the bus by an inherent controller, because the controller is essential for the system to generate the read clock 6:6-12 and address filter 120 on Fig. 3 ensures that the packet is delivered to appropriate buffer unit 2501-250N 5:15-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add an input control block, comprising an input memory unit, connected to each input port for buffering a data packet before transmitting the data packet over a distribution bus connected to all memory blocks corresponding to the input port and a third memory controller storing the packets into the input memory unit and reading them out over the bus of Takeuchi to the system of Yamazaki to improve the system reliability and speed by utilizing multiple memory blocks, as the packet can be redirected from the failed or overload memory block to the operational one.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dmitry Levitan whose telephone number is (571) 272-3093. The examiner can normally be reached on 8:30 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DL

Dmitry Levitan
Patent Examiner.
10/26/05

JOHN PEZZLO
PRIMARY EXAMINER